AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph beginning at page 1, line 22, with the following rewritten paragraph:

In recent years, it is well known that information electronics include a SOC (System On a Chip) (trademark) in which a system ~~including~~ includes a semiconductor memory device, a CPU (central processing unit), a plurality of input/output devices and the like, all of which are connected with each other via a bus, is built in one semiconductor chip. It is also well known that various methods for testing functions and performance of the above-described SOC have been developed. Particularly, a method for testing a semiconductor memory device mounted on the SOC is also well known. Such a method for testing a semiconductor memory device is disclosed, for example, in Japanese Patent Laid-Open No. Hei 7 (1995)-78495.

Please replace the paragraph beginning at page 2, line 9, with the following rewritten paragraph:

The semiconductor device of this example includes: a PLLC (Phase Locked Loop Circuit) 1; an AGC (Address Generating Circuit) 2; a DGC (Data Generating Circuit) 3; a synchronous RAM macro 4; a DC (Data Comparator) 5; and switches 6 to 10. The switches 6 to 10 are all turned on in a normal operation of the semiconductor device of this example and are all turned off in testing. In testing, the PLLC 1 generates an internal clock ICK having a frequency four times that of an external clock ECK. In ~~tenting~~ testing, the AGC 2 generates addresses of LSB two bits out of addresses A0 to An of n bits (n is a natural number) to be supplied to the RAM macro 4, in synchronization with the internal clock ICK.

Please replace the paragraph beginning at page 3, line 8, with the following rewritten paragraph:

The present inventor has recognized that storage capacity of the semiconductor memory device tends to increase year by year. Accordingly, a chip area is increased and miniaturization of a pattern is advanced. Thus, it has become more and more difficult to eliminate occurrence of

~~defect~~ defective memory cells incapable of writing and reading data in one semiconductor memory device.

Please replace the paragraph beginning at page 3, line 15, with the following rewritten paragraph:

In order to avoid the above-described problem, rescue of memory cells has been conventionally performed in the following manner. Specifically, extra rows and columns of memory cells (redundant memory cells) more than necessary storage capacity are provided in the semiconductor memory device and, in a probing test step of examining electrical characteristics and the like, a row including ~~defect~~ defective memory cells or a column including ~~defect~~ defective memory cells is replaced with the row of redundant memory cells or the column thereof. Thus, yield of the semiconductor memory device as a product has been improved.

Please replace the paragraph beginning at page 3, line 25, with the following rewritten paragraph:

In order to replace the above-described defect memory cells with the redundant memory cells, it is required to perform write and read of data for each of memory cells of the semiconductor memory device and determine whether the memory cell is a normal memory cell or a ~~defect~~ defective memory cell.

Please replace the paragraph beginning at page 4, line 21, with the following rewritten paragraph:

However, in the above-described probing test step, it is required to perform arithmetic processing as to which one of memory cells of which one of semiconductor memory devices formed on a semiconductor wafer is a ~~defect~~ defective memory cell and to store the result thereof in storage means called a fail memory.

Please replace the paragraph beginning at page 14, line 24, with the following rewritten paragraph:

When the test switch signal HSPT is "L" level, the connection switching circuit 18 shown in FIG. 2 supplies the RAM macro 12 with the external address EAD, the external clock ECK, the external write data [[TD]] ETD, the external chip select signal ECSB and the external write enable signal EWEB, which are supplied from the outside, as an address AD, a clock CK, write data TD, a chip select signal CSB and a write enable signal WEB, respectively. At the same time, the connection switching circuit 18 outputs the data read from the RAM macro 12 to the outside as the external read data TQ.

Please replace the paragraph beginning at page 15, line 19, with the following rewritten paragraph:

Based on the write enable signal WEB supplied from the connection switching circuit 18, the RAM macro 12 stores the write data TD supplied from the connection switching circuit 18 in a storage region corresponding to the address AD supplied from the connection switching circuit 18 in synchronization with the clock [[CD]] CK supplied from the connection switching circuit 18.

Please replace the paragraph beginning at page 15, line 25, with the following rewritten paragraph:

Moreover, in synchronization with the clock [[CD]] CK supplied from the connection switching circuit 18, the RAM macro 12 reads the read data TQ from the storage region corresponding to the address AD supplied from the connection switching circuit 18.

Please replace the paragraph beginning at page 16, line 20, with the following rewritten paragraph:

Next, a test method in the semiconductor memory device having the above-described configuration will be described. First, this test method will be schematically described with reference to timing charts shown in FIG. 6. After the test switch signal HSPT is set to "H" level

as shown in FIG. 6 (3), in a setting cycle TS, a pulse number n (n is a natural number) of the PLL clock PCK (see FIG. 6 (2)) is generated by the PLLC 14 per cycle of the external clock ECK shown in FIG. 6 (1), a method for generating the internal address IAD and a method for generating the internal write data ITD are set. As an example of this setting method, there is one in which, in a state where the test switch signal HSPT is "H" level and the external chip select signal ECSB is "H" level, the external write enable signal EWEB is set to "L" level, an address key is entered in the external address EAD and a mode entry is made by rise of the external clock ECK. Here, the method for generating the internal address IAD means any one of the following three patterns, for example: generating n number of internal addresses IADk (= EAD) (k is a natural number), IADk+1 (= EAD+1), ..., IADk+n-1 (= EAD+n-1) by sequentially increasing the address of the first given external address EAD; generating n number of internal addresses IADk (= EAD) (k is a natural number), IADk-1 (= EAD-1), ..., IADk-n+1 (= EAD-n+1) by sequentially decreasing the address of the first given external address EAD; and generating n number of internal addresses IAD0, IAD1, ..., IADk (= EAD) (k is a natural number), ... IADn-1 which include the first given ~~eternal~~ external address EAD and are separated every n number. Moreover, the method for generating the internal write data ITD means any one of the following four patterns, for example: consecutively generating n number of values of "1"; consecutively generating n number of values of "0"; repeating the values "1" and "0" alternately such as "101010..."; and repeating the values "0" and "1" alternately such as "010101....

Please replace the paragraph beginning at page 18, line 10, with the following rewritten paragraph:

In this write cycle TW, as shown in FIG. 6 (9), n bits of internal write data ITD are generated for one cycle of the external clock ECK in the high-speed data generating circuit 17 and these n bits of internal write data ITD are written into storage regions of the RAM macro 12 corresponding to the internal addresses IAD for n bits (see FIG. 6 (7)) which are generated in the high-speed address generating circuit 16. The generation of the internal write data ITD and the generation of the internal address IAD in this case are performed in accordance with the method for generating the internal write data ITD and the method for generating the internal address IAD,

which are set in the foregoing setting cycle TS. In FIG. 6 (9), "0 to n-1" indicates that n number of the internal write data ITD are generated in the high-speed data generating circuit 17 in accordance with the method for generating the internal write data ITD, which is set in the foregoing setting cycle TS. In FIG. 6 (7), the first "0 to n-1" from the left of the drawing indicates that n number of the internal addresses IAD are generated in accordance with the method for generating the internal address IAD, which is set in the foregoing setting cycle TS, are supplied to the RAM macro 12 via the connection switching circuit 18. Moreover, in FIG. 6 (12), the first "0 to n-1" from the left of the drawing indicates that n number of the internal addresses IAD are supplied to the RAM macro 12 from the high-speed address generating circuit 17 via the connection switching circuit 18 and write processing of n number of write data TD is performed in accordance with the n number of internal addresses IAD.

Please replace the paragraph beginning at page 22, line 17, with the following rewritten paragraph:

Meanwhile, in synchronization with rise of the PLL clock PCK, the internal address generating circuit 22 generates four internal addresses IAD ((0, 0), (1, 0), (2, 0) and (3, 0) in this case) (see FIG. 8 (6)) which ~~include~~ includes the external address EAD ([[(2, 0)]] (3, 0) in this case) supplied from the external address fetch/latch circuit 21 via the control bus 23 ~~(Step SP7)~~ (Step SP7)). Moreover, in the first and second read cycles TR1 and TR2 of the external clock ECK shown in FIG. 8 (1), in parallel with the above-described processing, the high-speed control signal generating circuit 15 generates the internal chip select signal ICSB and the internal write enable signal IWEB based on the external chip select signal ECSB and the external write enable signal EWEB. At the same time, based on the PLL clock PCK and the external address EAD, the high-speed control signal generating circuit 15 generates the read enable signal RE shown in FIG. 8 (7) (Step SP8).

Please replace the paragraph beginning at page 23, line 5, with the following rewritten paragraph:

Consequently, the four internal addresses IAD are supplied to the RAM macro 12 as four addresses AD ((0, 0), (1, 0), (2, 0) and (3, 0) in this case) via the connection switching circuit 18. Thus, four pieces of read data TQ are read from storage regions corresponding to the four addresses AD of the RAM macro 12 in synchronization with the clock CK supplied from the connection switching circuit 18 and are supplied to the high-speed data generating circuit 17 as four pieces of internal read data ITQ (4-bit data Q0 to Q3 in this case) (see FIG. 8 (8)) via the connection switching circuit 18 (Step SP9). In the high-speed data generating circuit 17, in the read data selecting circuit 24 shown in FIG. 4, the row address (Lx3, Lx2, Lx1, Lx0) included in the latch address LAD supplied from the external address fetch/latch circuit 21 and the row address (ix3, ix2, ix1, ix0) included in the internal address IAD supplied from the internal address generating circuit 22 are compared with each other. At the same time, the column address (Ly3, Ly2, Ly1, Ly0) included in the latch address LAD and the column address (iy3, iy2, iy1, iy0) included in the internal address IAD are compared with each other. When all bits of the row addresses and all bits of the column addresses coincide with each other, the selection signal RHIT of "H" level shown in FIG. 8 (9) is outputted from the 3-input AND gate 48 in synchronization with the PLL clock PCK. Therefore, from the transfer gate 55, only odd-numbered 1-bit data corresponding to the external address EAD ([[(2, 0)]] (3, 0) in this case) out of the four pieces of internal read data ITQ shown in FIG. 8 (8) is outputted.

Please replace the paragraph beginning at page 24, line 15, with the following rewritten paragraph:

Meanwhile, in synchronization with rise of the PLL clock PCK, the internal address generating circuit 22 generates four internal addresses IAD ((0, 0), (1, 0), (2, 0) and (3, 0) in this case) (see FIG. 8 (6)) which include the external address EAD ([[(3, 0)]] (0, 0) in this case) supplied from the external address fetch/latch circuit 21 via the control bus 23 (Step SP7). Moreover, in the first and second read cycles TR1 and TR2 of the external clock ECK shown in FIG. 8 (1), in parallel with the above-described processing, the high-speed control signal

generating circuit 15 generates the internal chip select signal ICSB and the internal write enable signal IWEB based on the external chip select signal ECSB and the external write enable signal EWEB. At the same time, based on the PLL clock PCK and the external address EAD, the high-speed control signal generating circuit 15 generates the read enable signal RE shown in FIG. 8 (7) (Step SP8).

Please replace the paragraph beginning at page 25, line 3, with the following rewritten paragraph:

Consequently, the four internal addresses IAD are supplied to the RAM macro 12 as four addresses AD ((0, 0), (1, 0), (2, 0) and (3, 0) in this case) via the connection switching circuit 18. Thus, four pieces of read data TQ are read from storage regions corresponding to the four addresses AD of the RAM macro 12 in synchronization with the clock CK supplied from the connection switching circuit 18 and are supplied to the high-speed data generating circuit 17 as four pieces of internal read data ITQ (4-bit data Q0 to Q3 in this case) (see FIG. 8 (8)) via the connection switching circuit 18 (Step SP9). In the high-speed data generating circuit 17, in the read data selecting circuit 24 shown in FIG. 4, the row address (Lx3, Lx2, Lx1, Lx0) included in the latch address LAD supplied from the external address fetch/latch circuit 21 and the row address (ix3, ix2, ix1, ix0) included in the internal address IAD supplied from the internal address generating circuit 22 are compared with each other. At the same time, the column address (Ly3, Ly2, Ly1, Ly0) included in the latch address LAD and the column address (iy3, iy2, iy1, iy0) included in the internal address IAD are compared with each other. When all bits of the row addresses and all bits of the column addresses coincide with each other, the selection signal RHIT of "H" level shown in FIG. 8 (9) is outputted from the 3-input AND gate 48 in synchronization with the PLL clock PCK. Therefore, from the transfer gate [[56]] 55, only even-numbered 1-bit data corresponding to the external address EAD ([[(3, 0)]] (0, 0) in this case) out of the four pieces of internal read data ITQ shown in FIG. 8 (8) is outputted.

Please replace the paragraph beginning at page 26, line 2, with the following rewritten paragraph:

Furthermore, in the data-out buffer circuit 25 shown in FIG. 4, the latch 64 latches the 1-bit data (the data Q2 in this case) outputted from the transfer gate 55. Meanwhile, in the read data selecting circuit 24, the data enable signal DE shown in FIG. 8 (11) is generated based on the external clock ECK and the read enable signal RE. Thus, in the data-out buffer circuit 25, the 1-bit data (the data Q2 in this case) latched by the latch 64 is outputted from the transfer gate [[66]] 67 opened by output data of the AND gate 62 synchronized with fall of the external clock ECK and is outputted as the external read data ETQ shown in FIG. 8 (12) after being inverted by the inverter 69 (Step SP10). Therefore, in an unillustrated test device, in synchronization with the external clock ECK, it is possible to determine in real time, based on the value of the external read data ETQ corresponding to the external address EAD one-on-one, whether one memory cell corresponding to the external address EAD of the RAM macro 12 is usable (pass) or not usable (fail).

Please replace the paragraph beginning at page 27, line 2, with the following rewritten paragraph:

Meanwhile, in synchronization with rise of the PLL clock PCK, the internal address generating circuit 22 generates four internal addresses IAD ((0, 0), (1, 0), (2, 0) and [[(0, 0)]] (3, 0) in this case) (see FIG. 8 (6)) which ~~include~~ includes the external address EAD ([[(3, 0)]] (1, 0) in this case) supplied from the external address fetch/latch circuit 21 via the control bus 23 (Step SP7). Moreover, in the third and fourth read cycles TR3 and TR4 of the external clock ECK shown in FIG. 8 (1), in parallel with the above-described processing, the high-speed control signal generating circuit 15 generates the internal chip select signal ICSB and the internal write enable signal IWEB based on the external chip select signal ECSB and the external write enable signal EWEB. At the same time, based on the PLL clock PCK and the external address EAD, the high-speed control signal generating circuit 15 generates the read enable signal RE shown in FIG. 8 (7) (Step SP8).

Please replace the paragraph beginning at page 27, line 18, with the following rewritten paragraph:

Consequently, the four internal addresses IAD are supplied to the RAM macro 12 as four addresses AD ((0, 0), (1, 0), (2, 0) and (3, 0) in this case) via the connection switching circuit 18. Thus, four pieces of read data TQ are read from storage regions corresponding to the four addresses AD of the RAM macro 12 in synchronization with the clock CK supplied from the connection switching circuit 18 and are supplied to the high-speed data generating circuit 17 as four pieces of internal read data ITQ (4-bit data Q0 to Q3 in this case) (see FIG. 8 (8)) via the connection switching circuit 18 (Step SP9). In the high-speed data generating circuit 17, in the read data selecting circuit 24 shown in FIG. 4, the row address (Lx3, Lx2, Lx1, Lx0) included in the latch address LAD supplied from the external address fetch/latch circuit 21 and the row address (ix3, ix2, ix1, ix0) included in the internal address IAD supplied from the internal address generating circuit 22 are compared with each other. At the same time, the column address (Ly3, Ly2, Ly1, Ly0) included in the latch address LAD and the column address (iy3, iy2, iy1, iy0) included in the internal address IAD are compared with each other. When all bits of the row addresses and all bits of the column addresses coincide with each other, the selection signal RHIT of "H" level shown in FIG. 8 (9) is outputted from the 3-input AND gate 48 in synchronization with the PLL clock PCK. Therefore, from the transfer gate [[56]] 55, only odd-numbered 1-bit data corresponding to the external address EAD ([[(0, 0)]] (1, 0) in this case) out of the four pieces of internal read data ITQ shown in FIG. 8 (8) is outputted.

Please replace the paragraph beginning at page 28, line 17, with the following rewritten paragraph:

Furthermore, in the data-out buffer circuit 25 shown in FIG. 4, the latch 64 latches the 1-bit data (the data Q3 in this case) outputted from the transfer gate 55. Meanwhile, in the read data selecting circuit 24, the data enable signal DE shown in FIG. 8 (11) is generated based on the external clock ECK and the read enable signal RE. Thus, in the data-out buffer circuit 25, the 1-bit data (the data Q3 in this case) latched by the latch 64 is outputted from the transfer gate [[66]] 67 opened by output data of the AND gate 62 synchronized with fall of the external clock

ECK and is outputted as the external read data ETQ shown in FIG. 8 (12) after being inverted by the inverter 69 (Step SP10). Therefore, in an unillustrated test device, in synchronization with the external clock ECK, it is possible to determine in real time, based on the value of the external read data ETQ corresponding to the external address EAD one-on-one, whether one memory cell corresponding to the external address EAD of the RAM macro 12 is usable (pass) or not usable (fail).

Please replace the paragraph beginning at page 29, line 9, with the following rewritten paragraph:

As described above, according to the configuration of this embodiment, it is made possible to realize write and read of data into and from the RAM macro 12 at high speed in the test circuit 11 by use of the PLL clock PCK which is synchronized with the low-speed external clock ECK and has a frequency n times that of the external clock ECK. In addition, it is made possible to perform read of 1-bit data corresponding to the external address EAD one-on-one in synchronization with the external clock ECK. Therefore, it is possible to determine in real time whether one memory cell of the RAM macro 12 corresponding to the read 1-bit data is usable (pass) or not usable (fail). Thus, the above-described method for testing a semiconductor memory device can be used in the probing test step of examining electrical characteristics and the like of the RAM macro 12 and performing rescue of memory cells in which a row including ~~defect~~ defective memory cells or a column including ~~defect~~ defective memory cells is replaced with a row of redundant memory cells or a column thereof. Moreover, in the above-described method for testing a semiconductor memory device, write of n number of the internal write data ITD is performed in synchronization with the high-speed PLL clock PCK only by supplying one external address EAD to the test circuit 11. Thus, a test time can be accordingly shortened.